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ABSTRACT

A decoder circuit according to the present invention comprises a global row decoder consisted of a first decoding means selected according to a row address signal and a second decoding means to which an output signal of the first decoding means and an erasure signal are input and a local row decoder for selecting each global word line signal outputted from the global row decoder. The local row decoder is consisted of a first and second transistors to the word line signal is input, and a third, fourth and fifth transistors outputting a first voltage supply signal and a second voltage supply signal to a sector word line